

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

Claim 1 (Currently Amended) A metal oxide semiconductor (MOS) device comprising:
a semi-conducting substrate having source and drain regions;
a gate dielectric of less than 100 Å thickness on said semi-conducting substrate, said gate dielectric is selected from the group consisting of HfO₂, ZrO₃, Y₂O₃, silicates or nitrogen additions of HfO₂, ZrO₃, or Y₂O₃, and mixtures thereof; and
a gate formed of a metal comprising Re on top of vertically abutting said gate dielectric, said gate comprising Re has an interface trapped charge density of about 3E 10 cm⁻² eV⁻¹ to about 4E 10 cm⁻² eV⁻¹, and wherein said Re is derived from a Re₂(CO)₁₀ CVD precursor.

Claim 2 (Previously Presented) A metal oxide semiconductor device according to claim 1, wherein said gate dielectric has a thickness of less than 50 Å.

Claim 3 (Cancelled)

Claim 4 (Cancelled)

Claim 5 (Cancelled)

Claim 6 (Cancelled)

Claim 7 (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is p-type or n-type.

Claim 8 (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs, and organic semiconductors.

Claim 9 (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of silicon.

Claim 10 (Currently Amended) A field effect transistor (FET) comprising:
a semi-conducting substrate having at least one source and one drain region;
a gate dielectric layer of less than 100 Å thickness on said semi-conducting substrate,
said gate dielectric layer is selected from the group consisting of HfO₂, ZrO₃, Y₂O₃, silicates or nitrogen additions of HfO₂, ZrO₃, or Y₂O₃, and mixtures thereof; and
a gate formed of a metal comprising Re ~~on top of vertically abutting~~ said gate dielectric layer, said gate comprising Re has an interface trapped charge density of about 3E 10 cm⁻² eV⁻¹ to about 4E 10 cm⁻² eV⁻¹, and wherein said Re is derived from a Re₂(CO)₁₀ CVD precursor.

Claim 11 (Previously Presented) A field effect transistor according to claim 10, wherein said gate dielectric layer has a thickness of less than 50 Å.

Claim 12 (Cancelled)

Claim 13 (Cancelled)

Claim 14 (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is p-type or n-type.

Claim 15 (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs, and organic semiconductors.

Claim 16 (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of silicon.

Claim 17 (Currently Amended) A metal oxide semiconductor (MOS) device comprising:
a semi-conducting substrate having source and drain regions;

a Hf-based gate dielectric of less than 100 Å on said semi-conducting substrate; and
a gate formed of a metal comprising Re on top of vertically abutting said Hf-based gate
dielectric, said gate comprising Re has an interface trapped charge density of about $3E\ 10\ cm^{-2}$
 eV^{-1} to about $4E\ 10\ cm^{-2}\ eV^{-1}$, and wherein said Re is derived from a $Re_2(CO)_{10}$ CVD precursor.